

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1278	716/6	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:09
L2	1611	716/5	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:09
L3	2048	716/4	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:09
L4	1	(716/6).ccls. and (soft adj error) and (timing adj analy\$)	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:11
L5	0	(716/5).ccls. and (soft adj error) and (timing adj analy\$)	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:11
L6	0	(716/4).ccls. and (soft adj error) and (timing adj analy\$)	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:11
L7	1	("716"/\$).ccls. and (soft adj error) and (timing adj analy\$)	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:12
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L10	0	(soft adj error) and (timing adj analy\$) and (design adj chang\$3)	US-PGPUB; USPAT	OR	OFF	2005/05/26 12:15
L11	4529	(soft error) and (timing analy\$) and (design chang\$3)	EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/26 12:15
L12	0	(soft adj error) and (timing adj analy\$) and (design adj chang\$3)	EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/26 12:16
L13	1	(soft adj error) and (timing adj analy\$)	EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/26 12:17
L14	27116	(soft error) and (timing analy\$)	EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/05/26 12:17



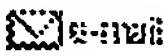
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- ☐
- 1. An on-chip ECC circuit for correcting soft errors in DRAMs with trench capacitor**
Mazumder, P.;
Solid-State Circuits, IEEE Journal of
Volume 27, Issue 11, Nov. 1992 Page(s):1623 - 1633
[AbstractPlus](#) | Full Text: [PDF\(760 KB\)](#) IEEE JNL

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2. Design for reducing alpha-particle-induced soft errors in ECL logic circuitry
Okabe, M.; Tatsuki, M.; Arima, Y.; Hirao, T.; Kuramitsu, Y.;
Solid-State Circuits, IEEE Journal of
Volume 24, Issue 5, Oct. 1989 Page(s):1397 - 1403
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3. Historical trend in alpha-particle induced soft error rates of the Alpha™ microprocessor
Seifert, N.; Moyer, D.; Leland, N.; Hokinson, R.;
Reliability Physics Symposium, 2001. Proceedings. 39th Annual. 2001 IEEE International
30 April-3 May 2001 Page(s):259 - 265
[AbstractPlus](#) | Full Text: [PDF\(632 KB\)](#) IEEE CNF

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4. A soft error immune 0.35 μm PD-SOI SRAM technology compatible with bulk CMOS
Ikeda, T.; Wakahara, S.; Tamaki, Y.; Higuchi, H.;
SOI Conference, 1998. Proceedings., 1998 IEEE International
5-8 Oct. 1998 Page(s):159 - 160
[AbstractPlus](#) | Full Text: [PDF\(196 KB\)](#) IEEE CNF

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5. High soft-error tolerance body-tied SOI technology with partial trench isolation (I²L) generation devices
Hirano, Y.; Iwamatsu, T.; Shiga, K.; Nii, K.; Sonoda, K.; Matsumoto, T.; Maeda, S.; Yan
Ipposhi, T.; Maegawa, S.; Inoue, Y.;
VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on
11-13 June 2002 Page(s):48 - 49
[AbstractPlus](#) | Full Text: [PDF\(401 KB\)](#) IEEE CNF

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6. Soft-error characteristics in bipolar memory cells with small critical charge
Idei, Y.; Homma, N.; Nambu, H.; Sakurai, Y.;
Electron Devices, IEEE Transactions on
Volume 38, Issue 11, Nov. 1991 Page(s):2465 - 2471
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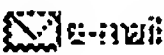
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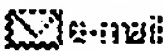
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Anghel, L.; Alexandrescu, D.; Nicolaidis, M.;
Integrated Circuits and Systems Design, 2000. Proceedings. 13th Symposium on
18-24 Sept. 2000 Page(s):237 - 242

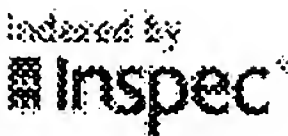
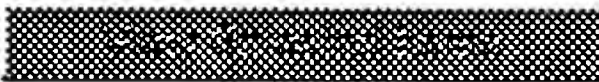
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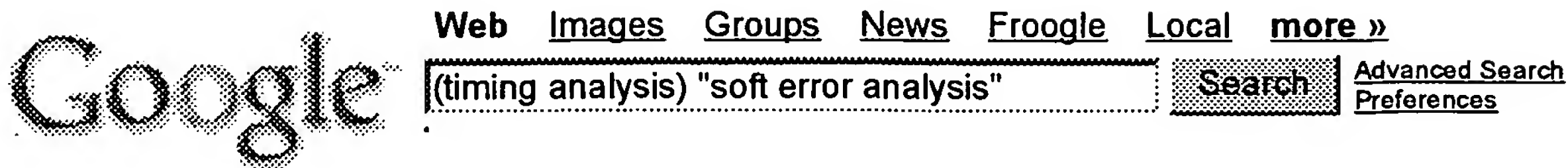
2. ICCAD 2004. International Conference on Computer Aided Design (IEEE Cat. No. 04CT12)
Computer Aided Design, 2004. ICCAD-2004. IEEE/ACM International Conference on
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The Soft Error Solution, iRoC Technologies

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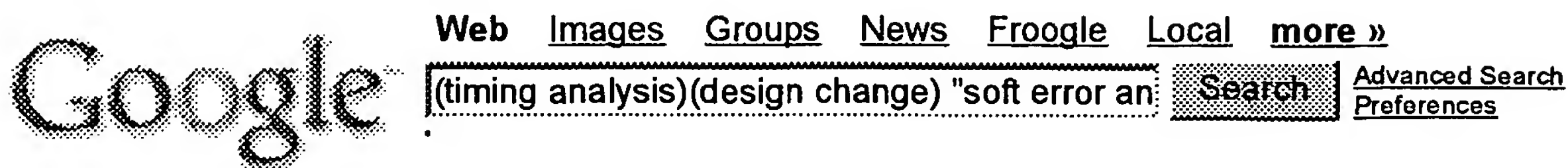
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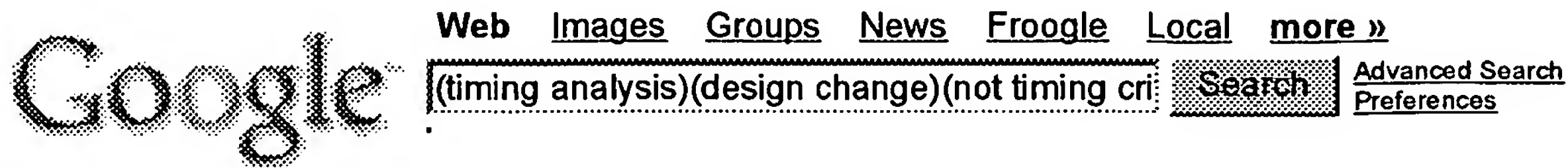
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